REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated October 20, 2005. Appreciation is expressed for the allowance of claims 34-36 and 40-42. By the present Amendment, new dependent claims 43 and 44 have been added to define further aspects of the present invention, as will be discussed below.

Briefly, the present invention defined by claims 37 and 39, as well as new dependent claims 43 and 44, is directed to an arrangement wherein a second silicon oxide film, such as 109 shown in Fig. 2B, as well as Fig. 5B, is formed so as to serve on an interpoly film for a non-volatile memory device (e.g., the memory cell region on the left side of Fig. 2, in which the film 109 is the interpoly film between the control gate 110 and the floating gate 107b) and also serves as a second portion of a gate insulating film for a field effect transistor (shown, for example, as the FET in the right hand portion of Fig. 2B in the high voltage region). More specifically, in the FET, as shown in the example of Fig. 2B, the gate insulating film for the FET is a laminated two layer structure formed of the insulator 108a (e.g., Fig. 2A) and the overlay insulator 109 (e.g., Fig. 2B). Incidentally, it is noted that the specific references to the figures is solely for purposes of example, and not intended to limit the claimed invention only to the specific details of these particular figures.

Reconsideration and removal of the 35 USC §103 rejection of independent claim 37 and its dependent claim 39 over the combination of Crivelli in view of Krivokapic is respectfully requested. Regarding this, claim 37 defines the above noted features shown, for example, in Fig. 2B in terms of:

> "forming a first silicon oxide film, which becomes a first portion of said gate insulating film, on the semiconductor substrate surface in the field effect transistor formed region by thermal oxidation method;
>
> depositing a second silicon oxide film which becomes said interpoly dielectric film and a second portion of said gate insulating film."

As such, the structure such as shown in Fig. 2B where a silicon oxide layer 109 forms both an interpoly film for a nonvolatile memory cell region and a second portion of a gate insulating film for a peripheral field effect transistors is clearly defined by the independent claim 37.

In Crivelli, on the other hand, no equivalent for this claimed second silicon oxide film having these multiple structural features, particularly the feature that it becomes the second portion of a gate insulating film for an FET, is even remotely suggested. Quite to the contrary, in Crivelli, as discussed on column 3, line 48 et seq., the gate insulating film 15 shown, for example, in Fig. 4 is clearly only a single layer insulating film. There is no teaching or suggestion whatsoever of this gate insulating film serving as a second layer for a gate insulating film of field effect transistors. Further, nothing in the secondary reference to Krivokapic teaches or suggests anything that would suggest the complete redesign of Crivelli which would be required to arrive at the claim structure. Accordingly, reconsideration and allowance of independent claim 37 and its dependent claim 39 over the combination of Crivelli and Krivocapic is respectfully requested.

In addition, the allowance of dependent claims 43 and 44 is also respectfully requested. These claims even more specifically define the distinguishing structure of the gate insulating film arrangement of the present invention, and, as such, the distinctions over the cited prior art. More specifically, these claims define the specific laminated structural arrangement of the gate insulating film with the second portion

being formed over the first portion. This clearly corresponds to the arrangement shown in Fig. 2B where the second portion defined in claims 43 and 44 can be read on the upper insulating film 109, while the first portion can be read on the lower insulating film 108a. As noted above, Crivelli completely lacks any teaching or suggestion of such a laminated structure utilizing two insulating films for the gate insulator of a field effect transistor. Similarly, nothing in the Krivokapic reference at all suggests this either. Accordingly, reconsideration and allowance of these new dependent claims 43 and 44, together with their parent claims 37 and 39, is earnestly solicited.

With regard to the gate insulating film of the field effect transistor having first and second portions, as defined in claim 37, and the laminated arrangement of these first and second portions, as defined in claims 43 and 44, it is noted that the Office Action attempts to meet the conditions of claim 37 as follows:

> "A first silicon oxide film (15) is formed on the semiconductor substrate surface which becomes a first portion of the gate insulating film (15). A second silicon oxide film (16) is deposited which becomes the interpoly dielectric film (15) and a second portion of the gate insulating film (15). "

It is respectfully submitted that a close examination of the description of the layers 15 and 16 in Crivelli (as well as the illustration of them) clearly indicates that this is actually not the case. To begin with, the first silicon oxide film 15, as shown in Figs. 5-8, is formed in the HV transistor region and the EPROM region. The insulating 15 is apparently not formed in the LV transistor section. This is clear, first of all, from the fact that the layer 15 is not shown in Figs. 5-8 under the LV portion on the right hand side of the drawings. In addition, column 3, lines 66 et seq. of Crivelli states:

> "The other portions are those to be used for the LV transistors which, in order to be subject to thermal oxidation, are subjected (Fig. 5) to a suitable etching

> process to remove all the layers formed on them by the preceding operations."

Column 4, lines 2 et seq. go on to describe the formation of the layer 16 as follows:

> "The parameters in this stage of processing are selected in such a way as to form a layer 16 of silicon dioxide having the thickness required for the gate dielectric of the LV transistors (for example, 5nm)."

With regard to this, it is important to note that the layer 16 is only shown for the LV transistor on the right side of Figs. 5-8, and is not shown at all in the other areas of the HV transistor (on the left side of the figures) or in the EPROM area. As such, it is clear that there is no field effect transistor in the arrangement of Crivelli which includes both the first silicon oxide film 15 as a first portion and the second silicon oxide film 16 as a second portion. Quite to the contrary, Crivelli merely shows the use of a single layer insulating film 15 for the HV and EPROM transistors, in a single layer insulating film 16 for the LV transistors. As such, it is quite clear that Crivelli fails to meet the features required in claim 37 for a gate insulating film for a field effect transistors that has two separate insulating films serving as first and second portions of the gate insulating film or the laminated structure defined in the dependent claims 43 and 44.

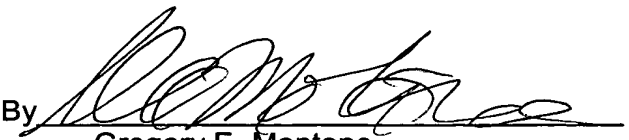
In conclusion on this point, it is noted that the only area of Crivelli which actually shows a superpositioning of insulating films is the area of the EPROM transistor in which the oxide film 15 is formed over the insulating film 12. However, this overlap of these insulating films is formed only over the source and drain regions, not under the gate 13a. Therefore, clearly, these overlapped insulating films 15 and 12 could not serve as a laminated gate insulating film structure. Further, this overlap is only for the EPROM area, and is not provided in the field effect transistor areas of the HV and LV transistors of Crivelli. As such, it is respectfully submitted

that there is absolutely no equivalent to the gate insulating film for a field effect transistor having first and second portions comprised of separate insulating films, as defined by claim 37, or the laminated structure for a gate insulating film for such field effect transistors defined by the dependent claims. Therefore, reconsideration and allowance of independent claim 37 and its dependent claims 39, 43 and 44 is earnestly solicited.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 500.39879VX1), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 
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